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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,803	12/29/2000	Wolfgang Roesner	AUS920000227US1	5327

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,803	ROESNER ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-10 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2,4-6,8-10 and 12 were amended.

2. Claims 3,7 and 11 were cancelled.

3. Claims 13-15 were added.

4. Claims 1-2, 4-6, 8-10 and 12-15 were examined.

Response to Applicant's Arguments

Amendments to Specification

5. Examiner acknowledges applicant's amendment to the specification.

35 USC § 112

6. Applicant's are thanked for addressing this issue. Examiner accepts applicant's answer. All 112 rejections are withdrawn.

35 USC § 102

7. Applicant's are thanked for addressing this issue. Rejection is withdrawn; however, upon further consideration, a new ground(s) of rejection is made in view of Swaboda et al.,(U.S. Patent 5,805,792 (1998)) and Gregory et al., (U.S. Patent 5,937,190 (1999)).

Final Rejection (2nd office action)

Drawings

8. Figure 1 represents a typical computer configuration (i.e., keyboard, mouse, etc), which encompasses the invention but was not created by the inventor. Therefore, figure 1 should be labeled as prior art.

Claim Rejections - 35 USC § 103

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-2, 4-6, 8-10, 12-15 are rejected under 35 U.S.C. 103 (a) as unpatentable by Swaboda et al.,(U.S. Patent 5,805,792 (1998)) in view of Gregory et al., (U.S. Patent 5,937,190 (1999)). Swaboda et al., teaches an electronic device having

addressable storage elements for bus accessibility; but doesn't teach HDL comment syntax. Gregory et al., teaches digital circuitry involving analyzing and debugging hardware description language (HDL). At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Gregory et al., by way of Swaboda et al., since it would be advantageous to annotate specific function within the model aid in the debugging process.

Claim 1. (Currently Amended) ((A)) In a computer-aided design and verification system a method for facilitating signal override (Swaboda: column 26, lines 13-20) in a simulation model of a digital circuit design (Swaboda: columns 2-3, lines 61-67 and 1-15, respectively) that includes one or more design entities described utilizing a hardware description language (HDL) (Gregory: columns 14-15, lines 45-67, and 1-10), said method comprising: instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax (Gregory: column 34, lines 48-57 with figure 31), said non-conventional HDL comment processed by a post-complier model build process (Gregory: columns 5-6 lines 57-67 and 1-36, respectively), wherein said non-conventional load tool instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler (Gregory: columns 5-6 lines 57-67 and 1-36, respectively) such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including: an input port map field containing

data representing an input port at which said instrumentation entity (Gregory: column 7, lines 9-19) receives a designated signal to be overridden (Swaboda: column 26, lines 13-20); and an output port mapping field comprising an override signal field specifying the name of said override signal (Swaboda: column 26, lines 13-20), a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden.

Claim 2. The method of claim 1 (Swaboda: column 26, lines 13-20; Gregory: columns 14-15, lines 45-67, and 1-10) wherein said output port mapping field further comprises a control port field specifying an output port for delivering an override enable signal (Swaboda: column 26, lines 13-20) to said signal selection means.

Claim 4 The method of claim 2, (Swaboda: column 26, lines 13-20; Gregory: columns 14-15, lines 45-67, and 1-10) further comprising instantiating a latch within said simulation model, wherein said latch stores an override disable bit; and combining said override disable bit with said override enable signal (Swaboda: column 26, lines 13-20) within a logic gate to produce a combined selection signal that determines whether of not said signal selection means overrides said designated signal with said override signal.

Claim 5. In a computer-aided design and verification system, a system for facilitating signal override (Swaboda: column 26, lines 13-20) in a simulation model of a digital circuit design (Swaboda: columns 2-3, lines 61-67 and 1-15, respectively) that includes one or more design entities described utilizing a hardware description language (HDL), said system comprising: processing means for instantiating an instrumentation entity within at least one or said one or more deign entities using port mapping fields designated by a non-conventional HDL comment syntax (Gregory: columns 5-6 lines 57-67 and 1-36, respectively), said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process (examiner interprets optimization as post compiling: Gregory: columns 7 and 19, lines 9-19 and 7-16, respectively), wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including: an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden (Swaboda: column 26, lines 13-20); and an output port mapping field comprising an override signal (Swaboda: column 26, lines 13-20) field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output (Gregory: column 7, lines 10-19) from said instrumentation entity, and a target signal field specifying (Gregory: column 39, lines 10-16) the name of said designated signal to be overridden.

Claim 6. The system of claim 5, (Swaboda: column 26, lines 13-20; Gregory: column 7, lines 10-19; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) wherein said output port mapping field further comprises a control port specifying an output port for delivering an override enable (Swaboda: column 26, lines 13-20) signal to said signal selection means.

Claim 8. The system of claim 6, (Swaboda: column 26, lines 13-20; Gregory: column 7, lines 10-19; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) further comprising: processing means of instantiating a latch within said simulation model, wherein said latch stores an override disable bit (Inherent: Swaboda: column 26, lines 13-20); and processing means for combining said override disable bit with override enable signal within a logic gate to produce a combined selection signal that determines whether or not signal selection means overrides said designated signal with said override signal.

Claim 9. In a computer-aided design and verification system, a computer program product of facilitating signal override (Swaboda: column 26, lines 13-20) in a simulation model of a digital circuit design (Swaboda: columns 2-3, lines 61-67 and 1-15, respectively) that includes one or more design entities described utilizing a hardware description language (HDL), said computer program product including computer-executable instructions for performing a method comprising: instantiating an instrumentation entity within at least one of said one or more design entities using port

mapping fields designated by a non-conventional HDL comment syntax, (Gregory: columns 5-6 lines 57-67 and 1-36, respectively) said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during post-compile model build process, (examiner interprets optimization as post compiling: Gregory: columns 7 and 19, lines 9-19 and 7-16, respectively) wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including: an input mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to overridden (Swaboda: column 26, lines 13-20); and an output mapping field comprising an override signal specifying the name of said override signal, a port name field specifying the name of the port from which said override signal (Gregory: column 7, lines 10-19) is output from said instrumentation entity, and a target signal field specifying the name of said designated to be overridden.

Claim 10. The computer program product of claim 9, (Swaboda: column 26, lines 13-20; Swaboda: columns 2-3, lines 61-67 and 1-15, respectively; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) wherein said output port mapping field further comprises a control port field specifying an output port for delivering an overriding enable signal to said selection means.

Claim 12. The computer program product of claim 10, (Swaboda: column 26, lines 13-20; Swaboda: columns 2-3, lines 61-67 and 1-15, respectively; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) wherein said method further comprises: instantiating a latch within said simulation model (Swaboda: column 2, line 65 and column 26, lines 5-26), wherein said latch stores an override disable bit (Inherent: Swaboda: column 26, lines 13-20); and combining said override disable bit with said override enable signal within a logic gate produce a combined selection signal that determines whether of not said signal selection means overrides said designated signal with said override signal (Swaboda: column 26, lines 13-20).

Claim 13. The method of claim 1, (Swaboda: column 26, lines 13-20; Gregory: columns 14-15, lines 45-67, and 1-10) further comprising generating signal selection means within said simulation model for selectively overriding said designated signal with said override said responsive to said post-compiler instrumentation (examiner interprets optimization as post compiling: Gregory: columns 7 and 19, lines 9-19 and 7-16, respectively) load tool processing said port mapping fields.

Claim 14. (New) The system of claim 5, (Swaboda: column 26, lines 13-20; Gregory: column 7, lines 10-19; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) further comprising processing means for generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler

instrumentation load tool (examiner interprets optimization as post compiling: Gregory: columns 7 and 19, lines 9-19 and 7-16, respectively) processing said port mapping fields.

Claim 15. The computer program product of claim 9, (Swaboda: column 26, lines 13-20; Swaboda: columns 2-3, lines 61-67 and 1-15, respectively; Gregory: columns 5-6 lines 57-67 and 1-36, respectively; Swaboda: column 26, lines 13-20) wherein said method further comprises generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation (examiner interprets optimization as post compiling: Gregory: columns 7 and 19, lines 9-19 and 7-16, respectively) load tool processing said port mapping fields.

Conclusion

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. Fax number is 571-273-3715

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (571)272-1400

February 28, 2005

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER